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DEVELOPMENT OF APPARATUS FOR PERFORMING RAPID CAPACITANCE-VOLTA--ETC(U)

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This report discusses the design of a complete experimental system for the observation of radiation effects in metal-insulator-semiconductor (MIS) capacitors by use of a rapid, repetitive capacitance-voltage (C-V) measurement technique. The apparatus includes trigger and control-signal generators, bias voltage sources, a sample holder with temperature control and radiation dosimetry, and a high-speed sample capacitance monitor. In typical

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operation, this apparatus repetitively measures the C-V characteristics of an MIS capacitor at intervals spaced logarithmically in time from 0.1 ms to 800 s, after a radiation pulse. Characteristics and operating principles of the major system components are discussed and sample test results are presented.

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FIGURES

FIGURES (Cont'd)

1. INTRODUCTION

The major effect of ionizing radiation in an MIS (metal-insulator-semiconductor) device is the production and trapping of charge in the oxide insulating layer. This trapped charge alters the electric field at the oxide-semiconductor interface causing a change (threshold voltage shift) in the turn-on voltage for the device. Information regarding the distribution and number of trapped charges may be obtained from capacitance-voltage (C-V) measurements on the device or an equivalent three-layer structure (MIS capacitor), since the bias-dependent capacity of such a structure is related to the same field-induced semiconductor charge accumulation, depletion, and inversion processes that are responsible for operation of the field-effect devices.[1]

Following its generation by a radiation pulse, the trapped charge distribution in the oxide layer of an MIS device may undergo changes as a function of time as a result of various relaxation (or annealing) processes. These processes, which may include recombination, charge injection or charge redistribution, generally cause a reduction in the radiation-induced threshold voltage shift and may occur at very early times after, or even during, the radiation pulse. This effect has great significance for devices that may be required to operate shortly (e.g., milliseconds) after exposure to nuclear radiation, especially since most MIS devices and materials have been characterized for radiation hardness in steady-state radiation sources using measurement techniques that sample the device status minutes or hours after irradiation. Use of the results from such slow measurement techniques without consideration of the damage relaxation characteristics of a device may result in serious miscalculation of the device response in an operational environment.

In order to observe the annealing or relaxation effects, several investigators[2,3] have performed C-V and device threshold voltage measurements on SiO_2 gate insulator structures using fast repetitive C-V

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[1] *For a discussion and additional references, see S. M. Sze, Physics of Semiconductor Devices, John Wiley and Sons (1969).*

[2] *M. Simons and H. L. Hughes, Short-term Charge Annealing in Electron-irradiated Silicon Dioxide, IEEE Trans. Nucl. Sci. NS-18 (December 1971).*

[3] *D. H. Habing and B. D. Schafer, Room Temperature Annealing of Ionization Induced Damage in CMOS Circuits, IEEE Trans. Nucl. Sci. NS-20 (December 1973).*

or I-V (current-voltage) sweeps applied immediately following a short radiation pulse. This report describes the development and operation of a complete experimental system capable of performing such fast C-V measurements at high speeds and under a wide range of bias and sample environment conditions. In typical operation, this apparatus repetitively measures the C-V characteristics of an MIS capacitor at intervals spaced logarithmically in time from 0.1 ms to 8000 s after a radiation pulse. Characteristics and operating principles of the major system components are discussed and sample test results are presented.

2. DESIGN CONSIDERATIONS

The basic requirements that were established for a system for performing fast repetitive C-V measurements are (1) a high-intensity, short-pulse radiation source, (2) a timing or trigger source that can initiate measurements at specified intervals after a radiation pulse, (3) a voltage source that can apply the appropriate biases and fast voltage ramps to the MIS sample, (4) a means of following rapid changes in the MIS sample capacitance caused by the fast voltage ramps, (5) a means of recording and identifying the fast C-V curves as they are generated, and (6) a sample holder with provisions for monitoring radiation dose to the sample and controlling sample temperature.

In our experiments, the radiation sources available were the Harry Diamond Laboratories (HDL) FX-45 flash x-ray machine operated in electron-beam mode at 4.1 MV and the Armed Forces Radiobiological Research Institute (AFRRI) electron linear accelerator operated at ~12 MeV beam energy. Either machine could easily deliver sufficient (>50 krads(Si)) radiation dose to an MIS sample in a single pulse to produce readily observable radiation effects. Dual-beam oscilloscopes with cameras were used for recording the C-V curves. These oscilloscopes were readily available and could provide the necessary bandwidth and desired rapid access to the data for quick analysis during the experiments.

3. DESCRIPTION OF FAST C-V APPARATUS

3.1 Initial Configuration

The initial experimental configuration developed was similar to that employed by Simons and Hughes.[2] This apparatus (fig. 1) consisted of a trigger generator, a commercial capacitance meter operating at

[2] *M. Simons and H. L. Hughes, Short-term Charge Annealing in Electron-irradiated Silicon Dioxide, IEEE Trans. Nucl. Sci.* NS-18 *(December 1971).*

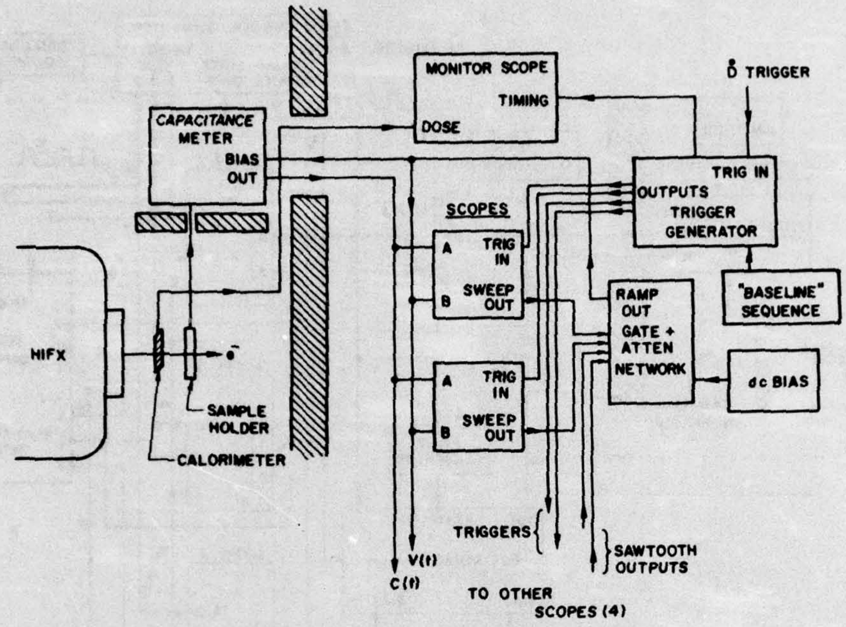

Figure 1. Fast C-V apparatus used for initial experiments.

1 MHz, a bias network, and six oscilloscopes. It was capable of generating C-V curves at logarithmically spaced times from 1 ms to 1000 s by using 1-ms-duration voltage ramps generated by the oscilloscopes and impressed upon constant bias levels. This setup was used for initial examinations of annealing in SiO_2 and Al_2O_3 capacitors. Useful results were obtained with this system, although it was cumbersome to set up and maintain in a calibrated state owing to the large number of oscilloscopes employed. It was also limited by the capacitance meter response to 1 ms or longer C-V sweep time and had no provision for independent variation of the C-V ramp bias and the pre- and postirradiation sample dc bias levels.

3.2 Advanced Configuration

The more advanced apparatus for observing fast annealing in MIS samples consists of four major subsystems: the control circuits, the bias supplies, the sample capacitance monitor, and the sample holder (fig. 2).

The control circuits include the trigger, baseline, staircase and blanking pulse generators. When triggered by the firing of the radiation source (flash x ray or LINAC), the trigger generator produces up to 24 pulses logarithmically spaced in time from 20 μs to 8000 s to

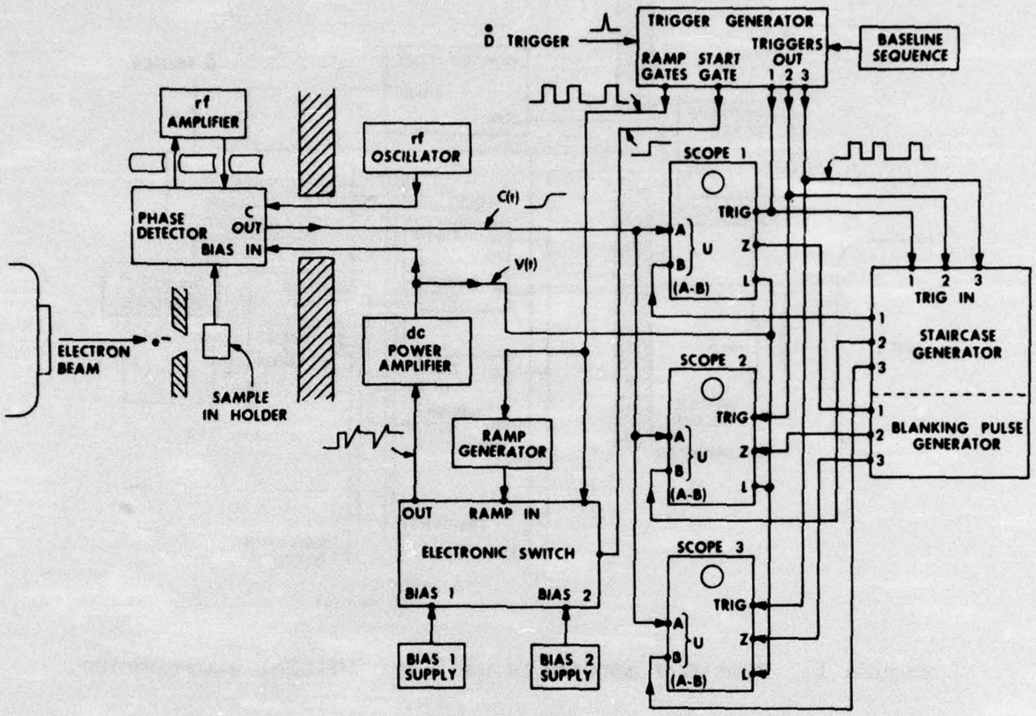

Figure 2. Improved fast C-V apparatus including bias control and trace identification.

initiate recording of a series of fast C-V measurements on as many as six oscilloscopes. The trigger pulses also actuate a staircase and blanking pulse generator that offsets and marks the successive sweeps on each scope for identification. Concurrent with the trigger pulses, the trigger generator produces a series of ramp gates and a bias control gate to actuate the fast electronic switch in the bias supply subsystem. Under control from the trigger generator, the bias supply generates the bias voltage that is applied across the MIS sample (refer to fig. 3). The preirradiation bias V_{gb}, the post irradiation holding bias V_{gh} and the amplitude and starting point of the ramp voltage used to obtain the C-V measurements may all be varied independently. Upon receipt of a radiation pulse the bias supply rapidly (<1 μs) switches from V_{gb} to V_{gh}. This bias is interrupted by the ramp triggers and 100-μs or 2-ms duration ramps are applied to the sample to generate the C-V curves. The capacitance monitor consists of a phase-sensitive detector operating at 3 to 150 MHz, which allows <2-μs resolution of a step change in sample capacitance. The MIS sample holder has provisions for electron-beam dosimetry and for maintaining the sample at a temperature in the range from 80 to 250 K.

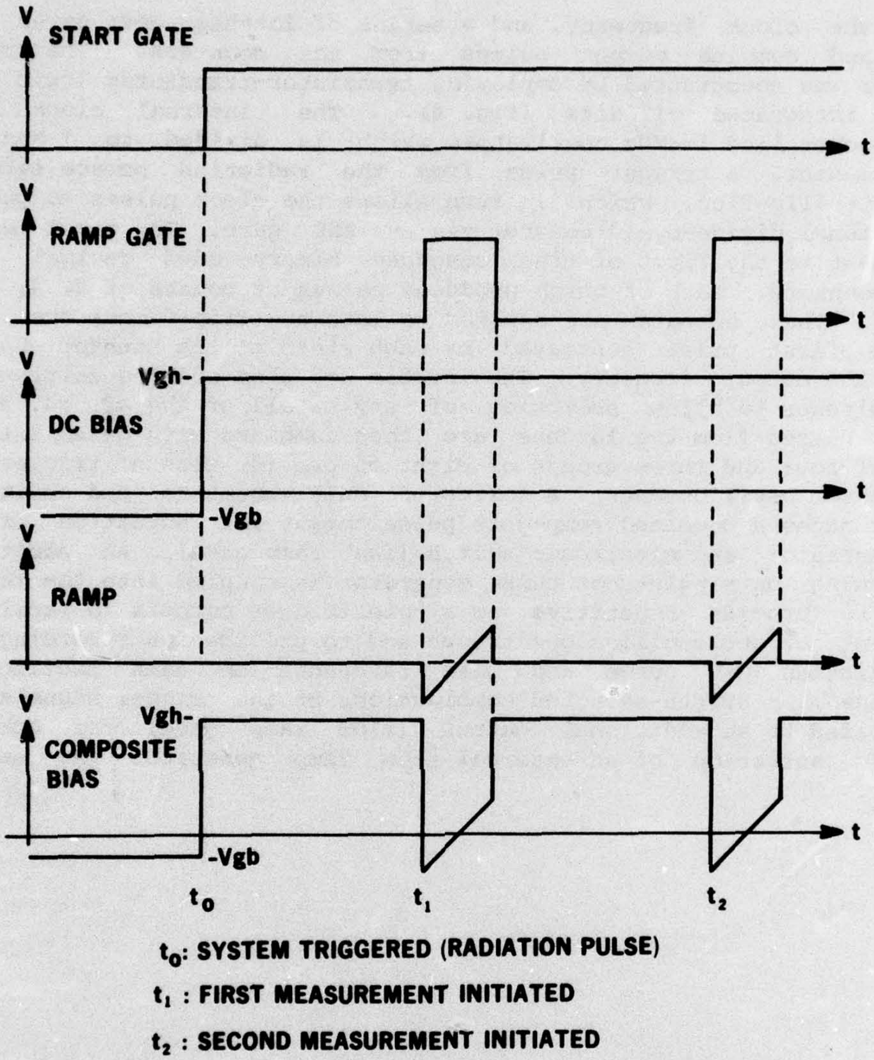

Figure 3. Generation of composite bias voltage.

3.2.1 Control Circuit

The control circuit generates the start gate, oscilloscope trigger pulses, ramp-gate pulses, staircase waveforms and blanking pulses at preset times after a radiation pulse. The primary unit--the trigger generator--consists of a clock that is gated on by a radiation detector when the radiation source fires, a series of counters that

divide the clock frequency, and a series of latches and gates that select and combine output pulses from the counters. The trigger generator was constructed by employing transistor-transistor logic (TTL) digital integrated circuits (fig. 4). The internal clock is a crystal-controlled 10-MHz oscillator, which is divided to 1 MHz by a decade counter. A trigger pulse from the radiation source sets the start gate flip-flop, which in turn allows the clock pulses to pass to an additional divide-by-10 counter via an AND gate. The gated 100-kHz pulses pass to the first of nine cascaded binary-coded decimal (BCD) decade counters, each of which produces pulses at counts of 2, 4, and 8 (fig. 5). These outputs are applied to latches (flip-flops) that allow only the first pulse generated by each state of the counter chain to pass to the output circuitry. The latches are also enabled in groups by panel switches to allow selection of any or all of the ×2, ×4, and ×8 counts. Pulses from the latches are then combined with gates into six groups of four and three groups of eight to provide sets of triggers for six or three oscilloscopes. A series of multivibrators and additional gates produces a combined ramp-gate pulse output for actuation of the ramp generator and electronic switch (fast ramp gate). An additional free-running or single-shot pulse generator is coupled into the trigger outputs to provide repetitive or single trigger outputs to facilitate adjustment of the oscilloscope traces and to provide for recording of a preirradiation C-V curve and bias reference on each oscilloscope ("baseline"). Switch-selected combinations of the trigger signals are also applied to an additional output (slow ramp gate) for optional automatic actuation of an external slow ramp generator and an X-Y recorder.

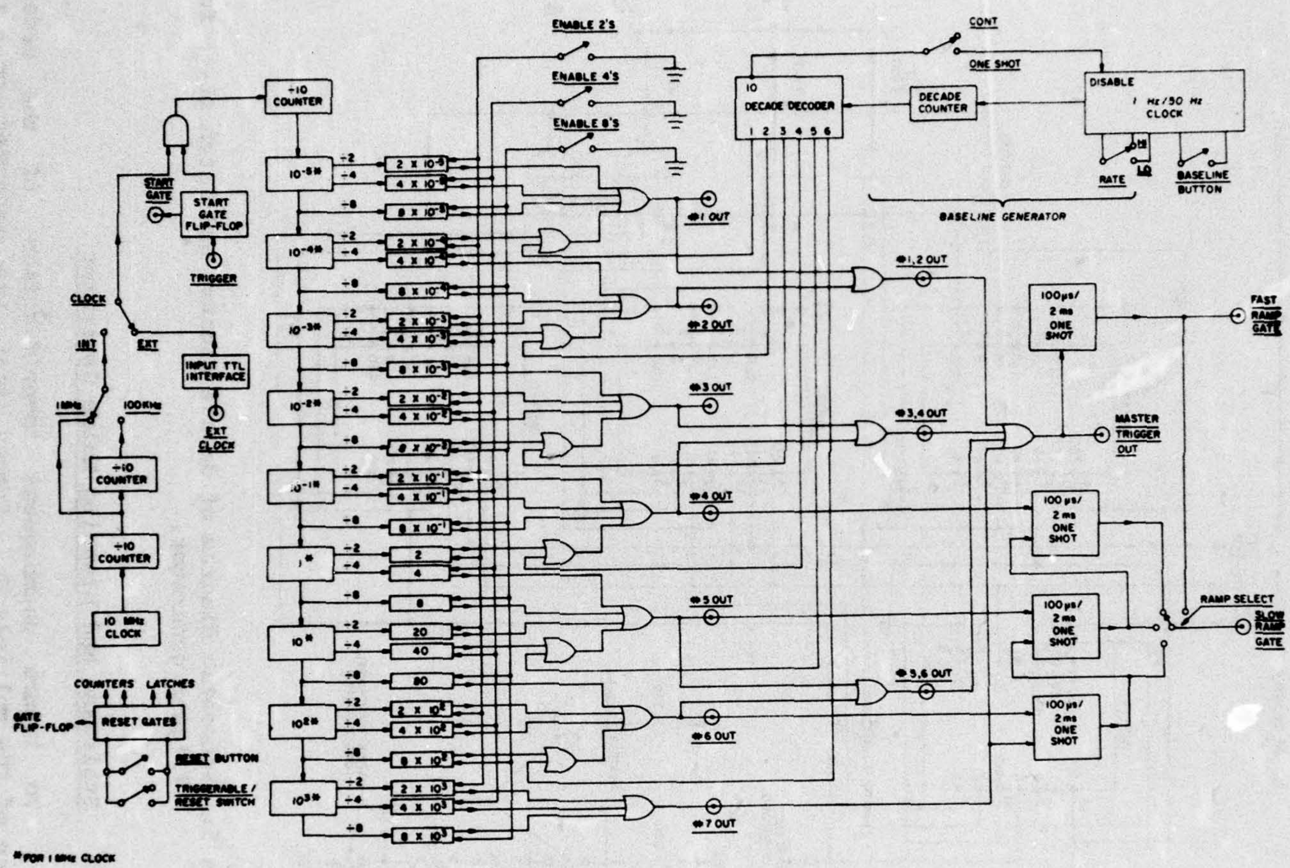

Figure 4. Block diagram of trigger generator.

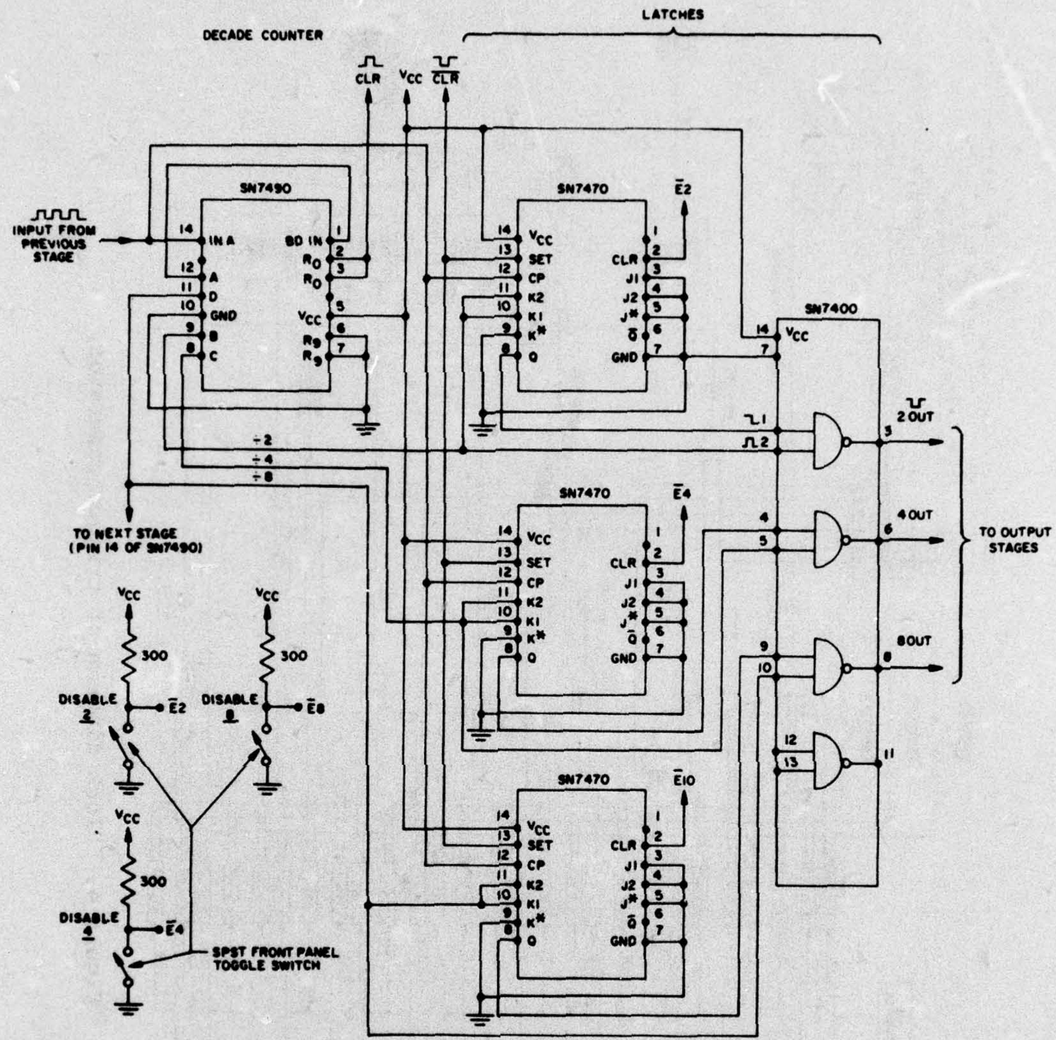

Figure 5. Schematic diagram of decade counter and latch stage for trigger generator.

3.2.2 Staircase and Blanking Pulse Generator

To insure unambiguous identification of the order of occurrence of the multiple C-V traces that are recorded on a single photograph during a test run (as many as eight pulses and baseline when three oscilloscopes are used), the traces are offset vertically and marked sequentially by a staircase and blanking pulse generator. This

unit consists of three identical subunits (fig. 6), each of which receives the trigger pulses for one scope and generates a staircase and blanking pulses for that scope. The staircase generator consists of a BCD counter, which increments upon termination of each C-V measurement ramp, and which drives a 2R-R resistive ladder network through its binary-coded outputs. The counter and the ladder form a 4-bit digital-to-analog converter. The converter staircase output is boosted by an operational amplifier. In use, this output is applied to the B channel of a differential (A-B) oscilloscope plug-in while the C-V signal is applied to the A channel, and the staircase amplitude is adjusted to give proper trace separation.

The sequential blanking pulses are obtained through use of another BCD counter and a 4-bit digital comparator. When a trigger pulse is received, an internal clock (a pair of RC cross-coupled gates) starts to generate pulses. These pulses are applied to the marker counter, which in turn has its outputs tied to the comparator "A" inputs. The comparator also monitors the trigger pulse count from the staircase BCD counter via its "B" inputs. When the marker count "A" exceeds the trigger pulse count "B," a blanking pulse is produced, the marker clock is disabled, and the marker counter is reset to zero to await the next trigger pulse. In use, the blanking pulses are amplified and applied to the Z-axis scope input. The result is production of a small gap in the oscilloscope trace, which is displaced to the right along the trace with respect to the gap in the preceding trace. This marker allows identification of the order of occurrence of the scope traces even if dc shift of the signal confuses trace identification by means of the staircase offset.

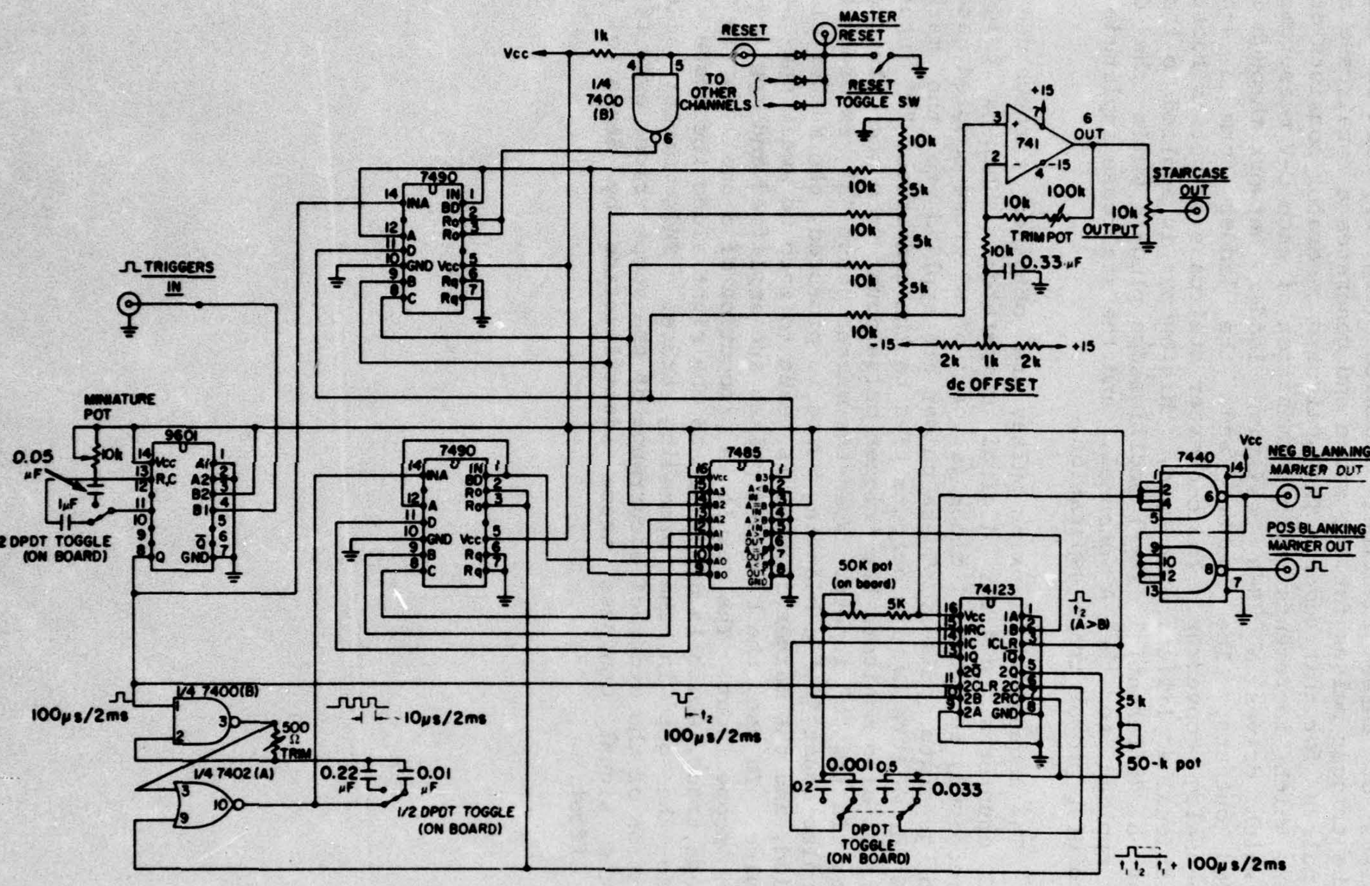

Figure 6. Schematic diagram of one channel of staircase/blanking pulse generator.

3.2.3 Bias Supplies

The bias supplies consist of two dc voltage sources, a ramp generator, a pair of electronic switches, and a dc amplifier. The voltage sources supply the adjustable steady pre- and postirradiation biases V_{gb} and V_{gh}. A current source and gated integrator together with an offset voltage source generate a 100-μs or 2-ms duration voltage ramp with adjustable amplitude and dc level (fig. 7). As illustrated in figure 3, the outputs of the bias and ramp sources are combined by a pair of electronic switches (fig. 8) to yield a composite bias voltage. Before a radiation pulse, the preirradiation bias source is connected to the output. When the radiation source fires, the trigger generator start-gate line goes high, causing the first electronic switch to connect the postirradiation bias source to the output. When a C-V curve is to be generated, the ramp-gate line from the trigger generator goes high, starting the integrator in the ramp generator and causing the second electronic switch to disconnect the postirradiation bias and connect the ramp and its dc offset to the output. When the ramp gate goes low, the ramp integrator is reset and the postirradiation bias is reconnected to the output. Switch transition times are about a microsecond.

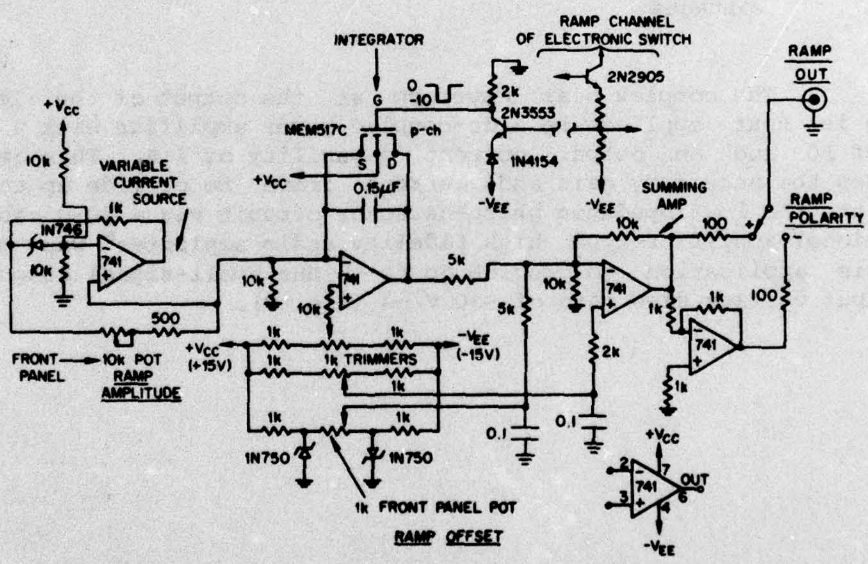

Figure 7. Schematic diagram of ramp generator.

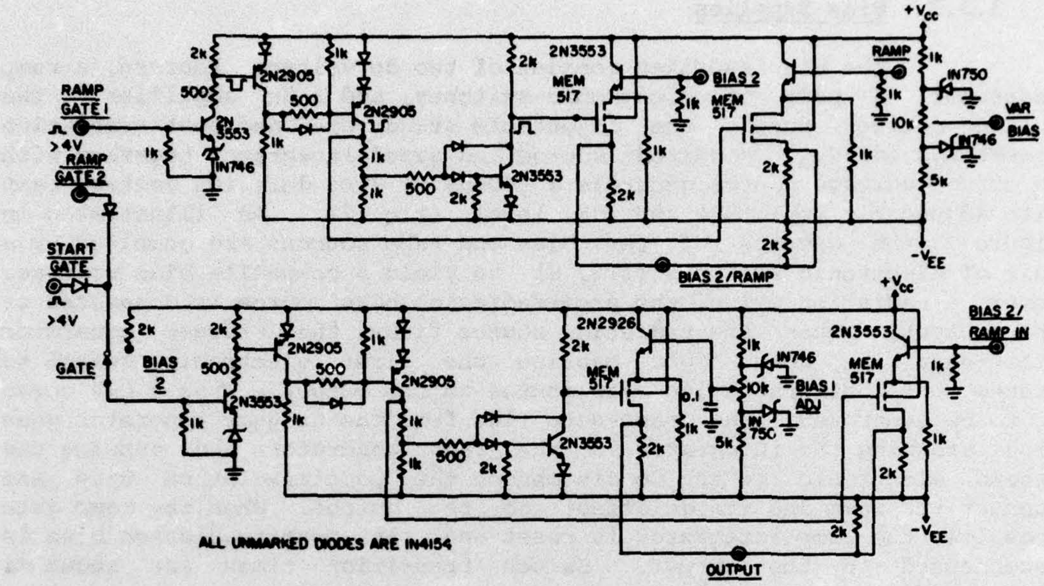

Figure 8. Schematic diagram of electronic switch for ramp and bias voltages.

The complex bias waveform at the output of the electronic switch is next applied to a dc-coupled power amplifier with a voltage gain of 10 and an output current capability of 1 A. This amplifier provides the necessary gain and current drive to provide up to ±45-V bias into the low-impedance phase-detector circuit via a 50-Ω cable. An operational-amplifier-type high fidelity audio amplifier[4] was modified for this application to provide dc to ~2-MHz small-signal response and an output voltage slew rate of ~20 V/μs (fig. 9).

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[4]*Original circuit described by D. Meyer, Assembling a Universal Tiger, Popular Electronics (July 1970).*

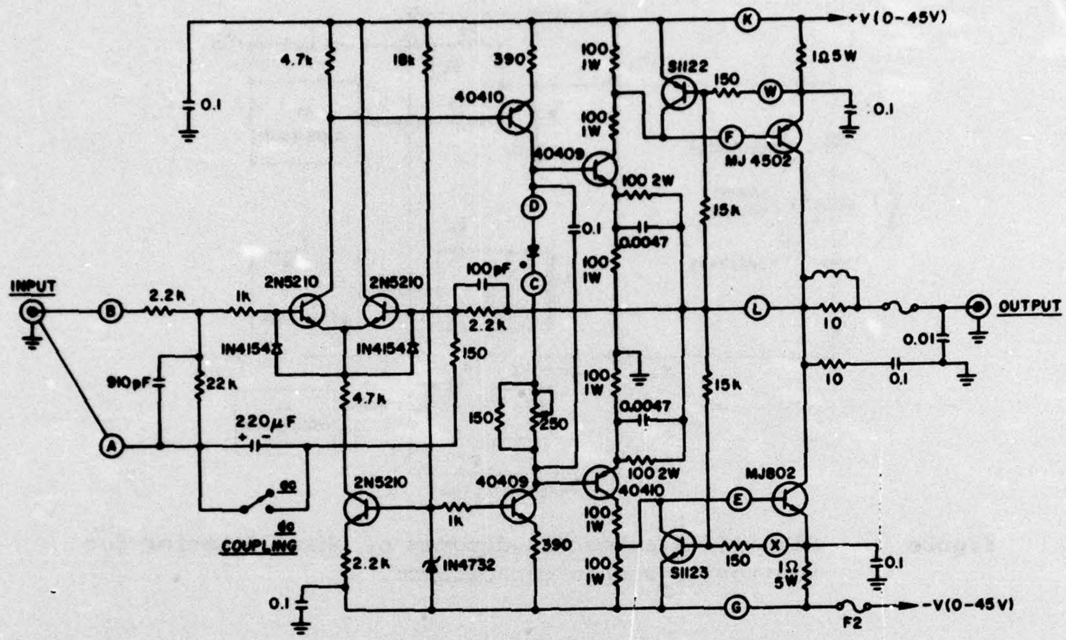


Figure 9. Schematic diagram of power amplifier for ramp and bias voltages.

3.2.4 Sample Capacitance Monitor

The sample capacitance as a function of time is measured by using a phase-sensitive detection technique (simplified schematic diagram, fig. 10). Bias and ramp voltages are applied to the sample via a low-pass filter (L_5, C_6). The 3- to 150-MHz rf probe frequency is applied to winding L_1 on the phase detector transformer. A portion $V(-C_x)$ (0.2 V peak-to-peak) of this signal is coupled out on L_2 and applied to the sample capacitance C_x. The rf current through C_x develops a signal voltage $V(+C_x)$ across the ac termination (R, C_4), which is coupled to the wide-band rf amplifier. After being amplified, the signal is delayed a precise amount and applied to the phase detector at D_1 and D_2. The dc voltage that appears at the junction of C_3 and L_4 is a function of the amplitude of the signal voltage on D_1 and D_2 and its phase relationship to the exciting or reference rf voltage on the detector transformer coupled into L_3 from L_1. The detector produces a maximum response for signals in phase with the reference and no response for signals in quadrature (± 90-deg phase relationship with the reference).

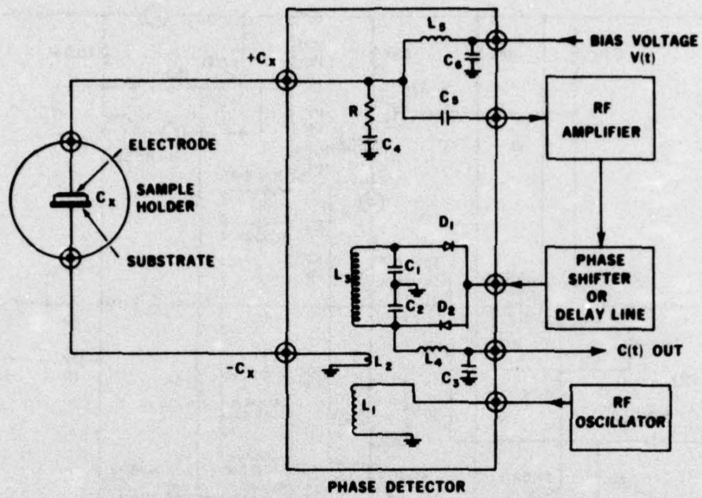


Figure 10. Simplified schematic diagram of phase detector for monitoring sample capacitance.

The admittance Y_x of C_x is given by $Y_x = G_x + j\,\omega\,C_x$ where G_x is the ac conductance of C_x and ω is the rf angular frequency. For $C_4 \gg C_x$ and $G_x \ll 1/R$, the rf signal $V(+C_x)$ across R is given by

$$V(+C_x) = \left[\left(RG_x + \omega^2R^2C_x^2\right) + j\omega RC_x\right] V(-C_x)/\left(1 + \omega^2R^2C_x^2\right)$$

If $\omega^2 R^2 C_x^2 \ll 1$, the reactive (imaginary) component of $V(+C_x)$ varies directly with C_x. Therefore, if the amplified signal from $-C_x$ is delayed correctly so that the phase-sensitive detector is responding only to its reactive component, the detector output will be proportional to C_x. For a typical experiment, $\omega = 6.28 \times 10^7\ s^{-1}$ (10 MHz), $R = 1\ \Omega$ and C_x may vary as a function of bias voltage from 100 to 400 pF. If the larger value for C_x is used, $\omega^2 R^2 C_x^2 = 6.32 \times 10^{-4} \ll 1$, the linearity condition is satisfied. Consequently, under these conditions the phase detector should produce a voltage output proportional to the sample capacitance as desired. The establishment of the proper phase relationship between the sample rf current signal and the reference signal in the phase detector is critical to proper operation of this capacitance measurement technique. At low (<10 MHz) frequencies a discrete-component phase shift network was used to obtain the necessary relationship; at higher frequencies, a delay line was used together with adjustments in operating frequency. Proper detector operation was

checked by switching a resistance in parallel with C_x (thereby increasing the in-phase or real signal component) and adjusting for minimum change in detector response. The detector could be calibrated to produce a known output voltage per unit sample capacitance. However, for most applications the experimental quantities desired (flat-band voltage and interface-state density) can be obtained from a normalized C-V curve and absolute calibration is not required.

3.2.5 Sample Holder

The sample holder used in the room-temperature measurements at the HDL Flash X-Ray (HIFX) facility consists of a collimator and sample block mounted on the end of the extendable 6-in.-diam electron drift tube. The collimator reduces the electron beam diameter to 0.25 in. immediately in front of the MIS sample to minimize unnecessary irradiation of leads or cable conduction. A thin (2-mil) copper calorimeter immediately in front of the sample provides shot-to-shot measurement of the pulsed electron fluence.

A more versatile sample holder, which allows measurements on MIS samples or devices over a wide temperature range, is in use at AFRRI. This unit (fig. 11) consists of a temperature-controllable sample mount built into a vacuum chamber, with provisions for admitting and collimating the irradiating electron beam. Low temperature control is accomplished by introducing liquid nitrogen or dry-ice-saturated acetone into a reservoir in the sample block. An electric heater provides high temperature control and sample temperature is monitored with a thermocouple. A small copper calorimeter is again employed for pulse-to-pulse electron beam dosimetry.

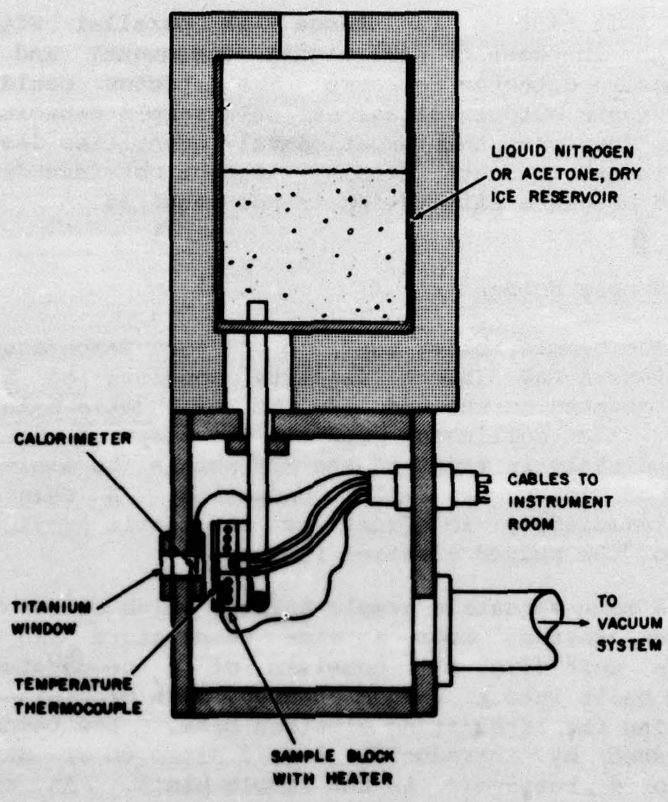
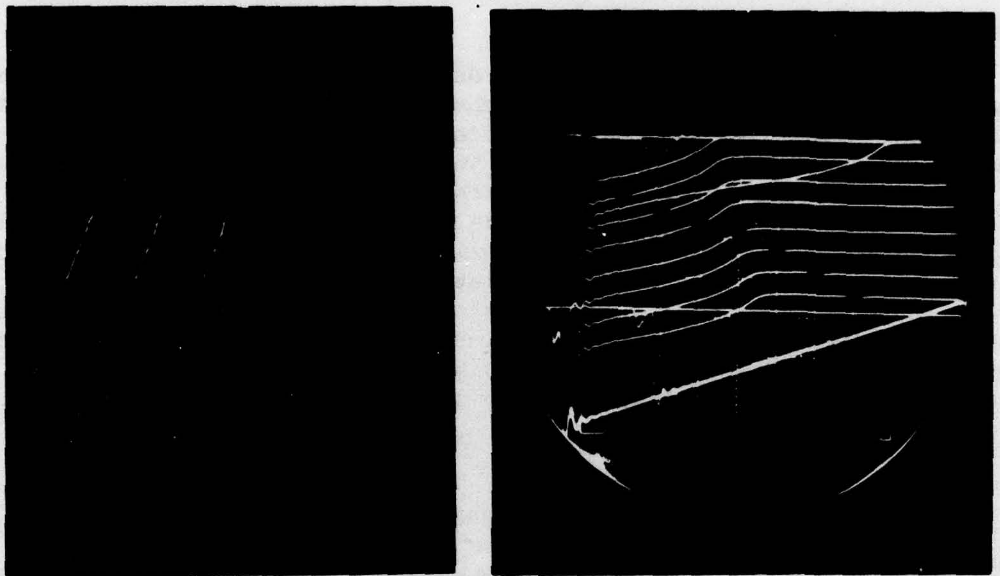


Figure 11. Sample holder for MIS sample with provisions for temperature control and electron-beam dosimetry.

4. TYPICAL FAST C-V RESULTS

Figure 12 show typical data taken with the apparatus in an experiment at HIFX. The lower traces in figure 12(a) show the calorimeter outputs from the radiation pulse and a baseline. The upper trace in figure 12(a) records the initial millisecond of the composite bias voltage applied to the sample following the radiation pulse. In this case, the steady bias was held at 0 V and the 100-μs ramps swept from -20 V to -5 V. Figure 12(b) shows the C-V data from one oscilloscope. The upper traces are the sample capacitance output from the phase detector with an accumulation capacitance reference (topmost horizontal line). The trace dropping down from the upper right is the preirradiation "baseline" sample capacitance characteristic; the eight left-shifted similar traces are the logarithmically spaced postirradiation curves offset and marked by the staircase generator (top



(a) (b)

Figure 12. Typical fast C-V data. (a) Upper trace: Bias voltage with ramps (2 V/cm vertical, 100 μs/cm horizontal). Lower trace: Thin Cu calorimeter output (50 μV/cm vertical, 2 ms/cm horizontal) (b) Upper traces: Sample capacitance Lower trace: Ramp voltage (5 V/cm vertical, 10 μs/cm horizontal, both beams).

to bottom in time sequence). The lower traces are the ramp voltage with its horizontal zero reference. Here the data are recorded as simultaneous readings of c(t) and v(t) rather than c(v) as is generally done in slower C-V measurements. While the oscilloscopes may be used in an X-Y mode, allowing direct recording of capacitance as a function of voltage, this requires recalibration and recentering of the horizontal amplifier each time the ramp voltage is altered. Also, the zero ramp voltage reference cannot be recorded if it lies outside the range of the ramp sweep (as in fig. 12(b)). In any case, c(v) is readily recovered from c(t) and v(t) by point-to-point correlation. The postirradiation curves in figure 12 show the usual leftward (i.e., negative voltage) displacement relative to the preirradiation curve that is associated with radiation-induced charge buildup in MIS structures. The progressive shift of the curves back toward the right (positive voltage shift) is evidence of relaxation of the radiation damage.

5. CONCLUSIONS

The apparatus that has been described was used for a series of experiments during FY74 on fast charge-injection and postirradiation annealing processes in metal oxide semiconductor (MOS) capacitors employing an Al_2O_3 gate insulator. These experiments yielded results that could be published within 6 months after the start of construction of the apparatus and demonstrated the importance of electron tunneling at the Al_2O_3 silicon interface.[5] During FY75 the apparatus was employed in a study of fast annealing of radiation-induced charge buildup in MOS capacitors with an SiO_2 gate insulator. These measurements established hole transport as the dominant factor in the annealing process.[6] Experiments are continuing and the C-V apparatus is undergoing futher modifications to accommodate additional experimental conditions and measurements.

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(3) D. H. Habing and B. D. Schafer, Room Temperature Annealing of Ionization Induced Damage in CMOS Circuits, IEEE Trans. Nucl. Sci. NS-20 (December 1973).

(4) Original circuit described by D. Meyer, Assembling a Universal Tiger, Popular Electronics (July 1970).

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